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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Gurley

In re Application of:	:	
Thomas G. Ference et al.	:	
Serial No.: 09/261,328	:	Art Unit: 2814
Filed: March 3, 1999	:	Examiner: D. Graybill
For: ULTRA-FINE CONTACT ALIGNMENT	:	Atty Docket: IBM – BU9-98-202 CBLH- 21806/0059

AMENDMENT FILED CONCURRENTLY WITH RCE UNDER 37 CFR §1.114

Commissioner for Patents
Washington, D.C. 20231

November 5, 2001

Sir:

In response to the Final Official Action dated June 5, 2001 and the Advisory Action dated October 2, 2001, the period for response having been extended for two (2) months until November 5, 2001, the following amendments and remarks are submitted in connection with the Request for Continued Examination filed under 37 C.F.R. § 1.114 in connection with the above-identified application.

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IN THE CLAIMS

Please amend claim 1 as follows:

1. (Amended) A semiconductor structure, comprising:

a first substrate;

a second substrate joined to the first substrate;

a plurality of contacts between the first substrate and the second substrate; and

a plurality of first solder bumps connected between the first substrate and the second substrate which align the plurality of contacts,

wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of contacts.

Please add the following new claims 54-59:

54. The semiconductor structure of claim 1, wherein the plurality of first solder bumps align a plurality of controlled collapse chip connection contacts.

55. A semiconductor structure, comprising:

a first substrate;

a second substrate opposing the first substrate;

a plurality of contacts between the first substrate and the second substrate; and

a plurality of first solder bumps connected between the first substrate and the second substrate which align the plurality of contacts,

wherein the plurality of first solder bumps are free of connection with any of the plurality of contacts.

56. The semiconductor structure of claim 55, wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of contacts.

57. The semiconductor structure of claim 55, wherein the plurality of first solder bumps align a plurality of controlled collapse chip connection contacts.

58. The semiconductor structure of claim 55, further comprising a ledge on the first substrate,

wherein all of the plurality of contacts are arranged on the ledge such that a lower surface of each of the plurality of contacts is coplanar with the ledge, and none of the plurality of first solder bumps are coplanar with the ledge, and

wherein an upper surface of each of the plurality of first solder bumps are essentially aligned with an upper surface of each of the plurality of contacts on a surface of the second substrate opposing the first substrate.

59. The semiconductor structure of claim 55, wherein the plurality of contacts comprise a plurality of second solder bumps each having a volume smaller than a volume of each of the plurality of first solder bumps.

REMARKS

Bearing in mind the comments of the Final Official Action, the Application has been amended so as to place it in condition for allowance. An early indication of the same would be greatly appreciated. Applicants point out that the Amendment after Final Rejection dated September 5, 2001 has not been entered with the filing of this RCE.

Claims 1-25 and 54-59 are pending in the present application. Claims 1 and 55 are independent. Claim 1 has been amended, and claims 54-59 have been added by the present Amendment.

Withdrawal of the rejection of claims 1-8, 10-18, 20, and 25 under 35 USC §102(b) as being anticipated by Akamatsu et al. (U.S. Patent No. 5,611,481) is requested.

It is noted that anticipation requires a disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 USC §102.[2] In view of the foregoing authority, the cited reference fails to anticipate claim 1, as amended.

Claim 1 has been amended to recite that the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of contacts. The applied art does not disclose this feature which, in exemplary embodiments, is shown in Figs. 1(a)-1(c) and 2. Accordingly, withdrawal of the rejection and allowance of amended claim 1 is requested.

As for dependent claims 2-8, 10-18, 20, and 25, these claims are submitted as defining patentable subject matter.

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[1] *Titanium Metals Corp. v Banner*, 227 USPQ 773 (Fed. Cir. 1985)
[2] *Scripts Clinic & Research Foundation v. Genentech, Inc.*, 18 USPQ 2d 1001 (Fed. Cir. 1991)

For example, with respect to claim 18, the applied art does not disclose "...a ledge on at least one of the first substrate and the second substrate, wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar."

Although the Official Action indicates that Akamatsu et al. discloses all features of Applicants recited invention, including the subject matter of claim 18, Applicants respectfully traverse this assertion. The Official Action offers electrode pad 5 as being equivalent to Applicants' recited ledge. While electrode pad 5 may arguably be viewed as a "ledge", electrode pad 5 in Akamatsu et al. does not reasonably disclose "a ledge on at least one of the first substrate and the second substrate, wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar, as recited in amended claim 1. Applicants' recited invention claims a plurality of contacts between the first substrate and the second substrate, and a plurality of first solder bumps connected between the first substrate and the second substrate which align the contacts.

In searching for disclosure in Akamatsu et al. which plausibly discloses a plurality of contacts and/or a plurality of first solder bumps, Applicants note the various embodiments of Akamatsu et al., including the embodiment, for example, disclosed in Figure 3. If electrode pad 5 is to be viewed as a ledge, an assertion that Applicants vigorously deny, electrode pad 5 does not disclose a ledge upon which all of the first solder bumps are arranged in contact with the ledge. If the assertion in the Official Action is to be taken at its face value, it appears that Akamatsu et al. discloses a plurality of ledges, each of which is associated with one of the plurality of first solder bumps.

To summarize, Akamatsu et al. in no way reasonably or fairly discloses a ledge, upon which the plurality of first solder bumps are arranged in contact, as recited in Applicants' original dependent claim 18.

Accordingly, withdrawal of the rejection and allowance of amended claim 1 are respectfully requested. Further, as dependent claims 2-8, 10-18, 20, and 25 are dependent on claim 1, each of these claims consequently incorporates the features and limitations of claim 1. Thus, these dependent claims are allowable over the applied art for at least the reasons described in connection with claim 1, as well as in their own right.

Further, in reliance upon the Examiner's indication in the Official Action dated November 3, 2000, that claim 1 is generic, consideration and allowance of previously non-elected species associated with dependent claims 7-9, 19, and 21-24 are also respectfully requested.

In order to establish a clear record, Applicants traverse the Examiner's assertion that Akamatsu et al. teach that the second bumps have a smaller size than the first bumps. The Examiner indicates his reliance upon asserted disclosure in Akamatsu et al. that the smallest width at the tip of the second bump is smaller than the width at the base of the first bump. Although this may arguably be true, as far as it goes, this assertion ignores the requirement that "[c]laims are read in the light of the disclosure of the specification on which they are based, not in a vacuum".[3]" As discussed in the specification, at least at page 10, line 16, the "...contacts may be smaller than the first solder bumps. Typically for example, ***the contacts may have a size, measured by diameter***, as small as about 20% of the diameter of the first solder bumps." (emphasis added).

Further, the Official Action indicates that, although Akamatsu et al. does not explicitly teach the particular dimensional limitations of Applicants' claims 10-15, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because Applicants have not disclosed that the dimensions are for a particular unobvious purpose, produced an unexpected result, or are otherwise critical, and it appear *prima facie* that the process would possess utility using other dimensions.

Applicants disagree with this assertion, as the specification discusses the necessary structure and alignment methodology required to achieve the fine alignment necessary for acceptable contact interconnection, particularly where much higher contact densities, compared to the conventional approach, of about 100,000 contacts/cm^2 are necessary. Such contact densities are desirable in "controlled collapse chip connection contacts" (C4) technology, for example. The dimensional limitations disregarded by the Examiner are discussed, with the requisite specificity in the specification, at least at page 11, lines 11 through page 12, line 3.

Applicants point out that the recited dimensional limitations are not a matter of obvious design choice, because the structure of the recited invention and the structure of Akamatsu et al. achieve different purposes. Akamatsu et al. is concerned with forming a soldering metal connection between a semiconductor chip and a circuit board which is free from the wetability problem related to the repellency of an aluminum inter connection layer against the melt of soldering metal. Akamatsu et al. is also concerned with forming a soldering metal connection that is free from disconnection failures caused by thermal stress.

In contrast, the present Application is concerned with providing a structure and method for joining two substrates in a semiconductor structure using the above-mentioned "controlled collapse chip connections", or "C4" connections, having self-aligning capabilities to ensure proper alignment of the two structures joined. Further, the present Application is directed to providing an order of magnitude or more improvement in the number of interconnects which can be joined. For example, the conventional limit for C4 interconnection technology which has a C4 connection diameter of about 50mm on a pitch of about 100mm, thus providing, for a chip having an area of about 1cm^2, at most about 10,000 C4 interconnects. In further contrast, the present Application allows a much greater number of interconnects compared with current C4 technology, e.g., 100,000 interconnects per square centimeter between the two chips, or more.

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[3] *In re Dean*, 130 USPQ 107,110 (CCPA 1961).

In similar circumstances relating to claims to an apparatus, "[t]he BPAI held that appellant had simply made an obvious design choice. However, the different structures of appellant and have the references achieved different purposes."[4] Further, "[t]o require an applicant to include in his specification evidence and arguments regarding whether particular subject matter was a matter of 'design choice' would be tantamount to requiring the Applicant to divine, before an application is filed, rejections the PTO will proper a finding of 'obvious design choice' is precluded where claimed structure and the function it performs are different from those of the prior art".[5]

Further, Applicants respectfully traverse the Examiner's contention that Akamatsu et al. teaches a plurality of first bumps connected between the substrate for lining the contacts. The Official Action asserts that Akamatus et al. teaches a plurality of first solder bumps for a connector between the substrates for aligning the contacts. Further, the Official Action points to Akamatsu et al. at column 4, lines 64-65, and column 6, lines 48-55 as explicitly teaching that the bump is for aligning the contacts. Applicants disagree with this assertion, as discussed below.

What is actually disclosed at the above-noted citations of Akamatsu et al., is that, in a manufacturing process, the first and second bumps are aligned to each other as shown in Figure 4D, then kept in contact with each other and heated at a connection temperature which is lower than a melting temperature of Indium. Applicants assert that this citation merely describes a manufacturing process wherein the bumps <u>are</u> aligned to each other, and not that the plurality of first solder bumps connected between the substrates are actually used in aligning the smaller contacts. It appears to Applicants that the only reasonable conclusion from the disclosure and structure of Akamatsu et al. is that the structure of Akamatsu et al. is acted upon by an external force to align first and second bumps.

[4] *In re Gal*, 25 USPQ 2d 1076, 1078 (Fed. Cir. 1992).
[5] *In re Chu*, 36 USPQ 2d 1089, 1095 (Fed. Cir. 1995).

Further, as for the asserted disclosure at column 6, lines 48-55, Akamatsu et al. merely discloses that the semiconductor chip 21, having an array of liquid connections 27A-27F, was mounted on circuit board 26 having an array of electrodes 25A-25F by flipping the semiconductor chip 21 so that the liquid connection to the semiconductor chip and the electrode on the circuit board were aligned to each other with a certain height, by maintaining a certain distance between the semiconductor chip and circuit board by spacer 28.

Again, Applicants respectfully submit that Akamatsu et al. does not teach a plurality of first solder bumps connected between the substrate for aligning the contacts. It seems fairly clear to Applicants that alignment of any bumps or contacts in Akamatsu et al. is accomplished by external means, and not by self-aligning capabilities resulting from surface tension in the solder in the C4 connections which draw the two structures together and align the connecting elements that the solder attaches to, as discussed in the present application.

The novel structure of Applicants' invention, as recited in amended claim 1 allows, for example, first solder bumps 5, having a larger diameter (as well as volume) than contacts 7, to roughly align the plurality of contacts, before fine-alignment of contacts 7 is accomplished.

In view of the above amendments and remarks, reconsideration and allowance of pending claims 1-25 in connection with the present application are respectfully requested.

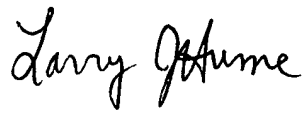
Newly presented claims 54-59 are submitted as being patentable, as they further define the invention using alternative claim language. Allowance of these claims is also requested.

Applicants believe that the present application is in condition for allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires clarification, the Examiner may contact the undersigned attorney so that this Application may continue to be expeditiously advanced.

Applicants respectfully petition for a two (2) month extension of time for responding to the Final Official Action. A check in partial payment of the extension of time fee is enclosed; the Commissioner is hereby authorized to charge any fees, or credit any overpayment, associated with excess claims and the remainder of the extension of time fee to IBM Deposit Account No. 09-0456.

Respectfully submitted,



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Enclosure: Claims after Amendment

Claims After Amendment

Please amend claim 1 as follows:

1. (Amended) A semiconductor structure, comprising:

a first substrate;

a second substrate joined to the first substrate;

a plurality of contacts between the first substrate and the second substrate; and

a plurality of first solder bumps connected between the first substrate and the second substrate [for aligning] which align the plurality of contacts,

wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of contacts.